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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,704	10/15/2003	Makoto Murata	Q77882	3647

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EXAMINER
NGUYEN, LINH M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

pD

Office Action Summary	Application No. 10/684,704	Applicant(s) MURATA ET AL.	
	Examiner Linh M. Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to Applicant's amendment filed 02/13/2006. Claims 1-6 are currently presented in the instant application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (U.S. Patent No. 6,326,826).

With respect to claim 1, Lee et al. discloses, in Fig. 1, clock generator comprising an input; an output; an oscillator [inherent clock source] that generates a reference clock [REF_CK], and a phase control means [11,12,13,14,15,19'] that receives the reference clock [REF_CK], controls a phase of the reference clock according to a variable setting condition at each clock cycle, and generates a phase controlled clock, comprising a phase comparator for comparing a phase of the reference clock with a phase controlled clock at the output, a first charge pump [15] for controlling a first current according to an output from the phase comparator, and a second charge pump for controlling a second current, and a delay setting circuit [11, 19'] that is responsive to the phase control means and generates an output, the second charge pump [14] that receives the output of the delay setting circuit *(via item 12),* wherein the phase control means varies a setting condition to spread a spectrum of the phase controlled clock outputted at the output.

With respect to claim 2, Lee et al. discloses, in Fig. 1, clock generator comprising a phase control means that receives a reference clock [REF_CK] and controls a phase of the reference clock according to a variable setting condition at each clock cycle, and generates a phase controlled clock, the phase control means comprising a variable delay circuit [11], a first charge pump [15] for controlling a first current, and a second charge pump [14] having a capacity larger than (col. 2, line 61 to col. 3, line 5) the first charge pump for controlling a second current, and, a delay setting circuit [11, 19'] for providing an output to the second charge pump [14], wherein the first and second currents are combined and supplied to the variable delay circuit as a control input, and wherein the phase control means varies a setting condition to spread a spectrum of the phase controlled clock outputted at the output.

With respect to claim 3, Lee et al. discloses, in Fig. 1, a variable delay circuit [11] that delays the reference clock [REF_CK] to comply with a control input according to the setting condition, and the phase control means includes a circuit [13] that detects a delayed state in the variable delay circuit, and regulates the control input to the variable delay circuit [11] in such a manner that a phase difference of the phase controlled clock to the reference clock does not exceed a specific limit value defined by the reference clock cycle as a unit.

With respect to claim 4, Lee et al. discloses, in Fig. 1, that the phase control means [11,12,13,14,15,19'] regulates the control input according to such a profile that the phase difference of the phase controlled clock to the reference clock gradually increases and gradually decreases between the upper limit and lower limit of the specific limit value defined by the reference clock cycle as a unit.

With respect to claim 5, Lee et al. discloses, in Fig. 1, that the phase control means [11,12,13,14,15,19'] comprises a DLL circuit containing the variable delay circuit [11] as a circuit element, in which the phase control means synthesizes the control input to the variable delay circuit [11].

With respect to claim 6, Lee et al. discloses, in Fig. 1 and col. 2, line 61 to col. 3, line 5, a clock generator comprising an input; an output; an oscillator [inherent clock source] that generates a reference clock [REF_CK] and a phase control means [11,12,13,14,15,19'] that receives the reference clock [REF_CK], controls a phase of the reference clock according to a variable setting condition at each clock cycle and generates a phase controlled clock, in which the phase control means varies a setting condition to spread a spectrum of the phase controlled clock outputted at the output, in which the phase control means includes (a) a variable delay circuit [11] that delays the reference clock [REF_CK] to comply with a control input according to the setting condition, (b) a circuit [12, 13] that detects a delayed state in the variable delay circuit and regulates the control input to the variable delay circuit in such a manner that a phase difference of the phase controlled clock to the reference clock does not exceed a specific limit value defined by the reference clock cycle as a unit and (c) a DLL circuit containing the variable delay circuit [11] as a circuit element, in which the phase control means synthesizes the control input to the variable delay circuit, and in which the variable delay circuit [11] delays the reference clock [REF_CK] based on a control voltage [output from 16]; the DLL circuit includes a comparator [12, 13] that compares the phase of a delayed output clock from the variable delay circuit and the phase of the reference clock, and a first charge pump that controls a first current and generates the control voltage to the variable delay circuit according to a phase difference output from the comparator; and the phase control means uses a second charge pump [14] of which capacity is greater than that (col. 2, line 61 to col. 3, line 5) of the first charge pump in a circuit for adjusting the control input, and generates the control voltage according to a phase difference set as a control condition.

Remarks

3. Applicant's arguments with respect to claims 1-6 have been considered but they are not persuasive.

With respect to Applicant's argument regarding claims 1, 2 and 6, on page 7, first paragraph, lines 1-2, the Applicant stated that "*there is no mention in Lee et al. of a manner of achieving a spread spectrum effect*". The examiner disagrees. First, as stated in MPEP § 2163.02, the subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement; and second, Lee discloses, in Fig. 1, generating a wide frequency range delay locked loop encompassing a plurality of delay elements 18' for outputting a multi-phase clock, the delay chain 11 comprises seven delay cells to generate a seven phase clock [col. 2, lines 44-51], each delay cell 19' comprises 2 inverters, whose outputs are controlled/set by a delay control signal which activates switches 8 and 9. Thus, Lee et al. does indeed discloses that the phase control means [11, 12, 13, 14, 15 and 19'] varies a setting condition to spread a spectrum of the phase-controlled clock outputted at the output.

In conclusion, the rejections set forth in the office action regarding claims 1-6 sustain.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER